DOCKET NO.: 98-MET-069 (STMI01-01012) **PATENT**
Customer No.: 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	David L. Isaman
Application No.	:	09/443,160
Filed	:	November 19, 1999
For	:	SYMBOLIC STORE-LOAD BYPASS
Art Unit	:	2183
Examiner	:	Alrobaye, Idriss N.
Confirmation No.	:	6854

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Appellant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

STATUS OF THE CLAIMS

Claims 2-3, 6-13, and 16-21 are pending.

Claims 2-3, 6-13, and 16-21 stand rejected.

REJECTIONS

Claims 2-3, 6-13, and 16-19 were rejected under 35 U.S.C. § 112 First Paragraph. Claims 2, 12 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,216,200 to Yeager (hereinafter "*Yeager*"). Claims 2-3, 6-13 and 16-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,666,506 to Hesson (hereinafter "*Hesson*").

REMARKS

The Examiner contends that the Specification does not explain or show the current claim language "without computing a memory address equaling the first base address value added to the offset address value in detecting the first instruction." The Examiner states that "[t]he specification does not show a memory address equaling **the first base address value added to the offset address value** is not computed in detected [sic] the first instruction. The Specification shows that the referenced external memory address is not computed (Specification page 4, lines 3-6) but there is not mentioning [sic] of "first base address value **added** to the offset address value." (*Advisory Action*, page 2). However, the Specification, starting at page 8, line 6, teaches that an effective address is computed by an address value added to an offset value. A first instruction can be computed from a base address value added to an offset address value, and stored. Thereafter, starting at page 9, line 9, a second instruction can be detected **without having to compute the effective address**. Therefore, the Specification, from page 8, line 6 through page 13, line 2, teaches that an instruction can be detected without computing a memory address, wherein a memory address equals the first address added to the offset value. The Examiner has failed to consider the full sequence of steps taught by the Specification. Accordingly, the contentions by the Examiner are factually deficient and the rejection is unsupported.

In the Advisory Action, the Examiner maintains the position that *Yeager* anticipates Claims 2, 12 and 20. However, the Examiner has failed to provide a reference that teaches, expressly or inherently, each and every element as arranged and recited by the claims of the instant application. Further, the Examiner has failed to put forth any arguments each and has not provided any articulated reason as to how any deficiency (missing element) could be solved in a predictable manner through combination with any other references.

Independent Claims 2 and 12 each specify "wherein the first instruction is detected based upon the first base and offset address values and without computing a memory address equaling the first base address value added to the offset address value in detecting the first instruction." Independent Claim 20 specifies "using the syntax for the first instruction and the syntax for the second instruction to determine a relationship between the first memory location and the second memory location, without using the effective address of the first memory location or the effective address of the second memory location to determine the relationship between the first memory location and the second memory location." These elements are not taught or suggested by *Yeager*, therefore the rejection is legally and factually deficient.

The Examiner appears to misinterpret the disclosure in *Yeager* with respect to these elements. The Examiner argues that *Yeager's* comparison of virtual addresses, as taught in col. 30, lines 43-49, is the same as "without computing a memory address equaling the first base address value added to the offset address values in detecting the first instruction." The Examiner states that "[t]here is no memory address computation equaling the first base address value added to the offset address values, thus reads on the limitation; see also abstract wherein the dependencies is detected before virtual address calculation." (*Office Action*, page 6).

Yeager, however, teaches that dependencies may be tracked based on a presumption and corrected once the actual address is computed. *Yeager* also teaches comparing virtual addresses that are, for indexed address calculations, formed by "base+index". (*Yeager*, col. 9, lines 21-22). *Yeager* expressly teaches that the virtual address is altered (e.g., an offset value) by a previous store, or a default is used and reset when the previous address is ultimately calculated. (*Yeager*, col. 30, line43

– col. 31, line 9). As such, *Yeager* teaches tracking a value using a default value until the actual address is calculated. Therefore, a calculation still must occur. The Examiner's interpretation of the teachings in *Yeager* is factually incorrect. The Examiners reliance on *Yeager* to teach each and every element as arranged and recited in Claims is legally deficient.

In regard to the rejection of Claim 20, the Examiner contends that there is no memory calculation, in *Yeager*, equaling the first base address value added to the offset address value. As stated herein above, *Yeager* requires a calculation. *Yeager* expressly teaches that "dependencies" may be tracked before actual calculation of the virtual address based on a "presumption of the dependency" and such dependency is dynamically corrected **once the address becomes available**. (*Yeager*, Abstract) The dependency is a relationship between an instruction and the operands produced by a prior instruction. (See generally, *Yeager*, col. 1, lines 29-33). Accordingly, the Examiner's contentions are factually deficient and the § 102(b) rejection is legally deficient.

Furthermore, the Examiner argues that *Hesson* teaches a virtual address that includes a base and offset address. However, no support exists in *Hesson* for this interpretation by the Examiner that the virtual address includes a base and offset address. The Examiner merely argues that the features upon which the Applicants rely (i.e., physical or real addresses) are not recited in the rejected claims. (*Advisory Action*, page 5). However, the Examiner fails to provide a citation illustrating where *Hesson* expressly or inherently teaches that a virtual address includes a base and an offset address. The Examiner's reliance on *Hesson* to teach wherein the first instruction is detected based upon the first base and offset address values and without using a memory address equaling to the first address value added to the offset address value is both factually and legally deficient.

In regard to Claim 20, the Examiner concedes that *Hesson* does not teach determining the syntax for the first instruction and the syntax for the second instruction without using the effective address. (*Office Action*, page 8). The Examiner merely offers a conclusory interpretation but has not shown where *Hesson* inherently teaches such. Therefore, the § 102(b) rejection of Claim 20 as anticipated by *Hesson* is legally deficient.

CONCLUSION

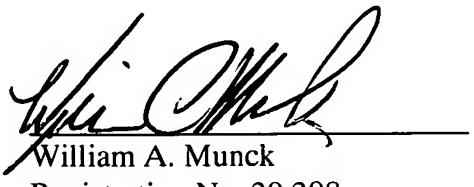
As a result of the foregoing, the Applicants assert that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

For the reasons given above, the Applicants respectfully request reconsideration and allowance of the pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP



Date: October 13, 2009

William A. Munck
Registration No. 39,308

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@munckcarter.com*